In the Claims

1. (Previously Presented) A charge pump fabricated on a substrate for use in a phase lock loop system, the charge pump comprising:

a first input stage having a first input transistor that receives a first control signal, a first complementary transistor, and a first discharging transistor,

where the source terminals of the first input transistor and the first complementary transistor are connected with a drain terminal of the first discharging transistor, and the first complementary transistor is operable to receive a first reference signal having a substantially constant voltage;

a second input stage coupled to the first input stage, the second input stage having a second switching transistor that receives a second control signal, a second complementary transistor, and a second discharging transistor,

where the source terminals of the second input transistor and the second complementary transistor are connected with a drain terminal of the second discharging transistor, and the second complementary transistor operable to receive a second reference signal having a substantially constant voltage;

a first output terminal for providing an output signal having reduced switching noise, the output terminal being coupled to the second complementary transistor;

a first charging transistor connected between a supply voltage and the first input transistor and a second charging transistor connected between a supply voltage and the second input transistor; and

a third charging transistor connected between the supply voltage and the first complementary transistor and a fourth charging transistor connected between the supply voltage and the second complementary transistor.

2. (Previously Presented) The charge pump of claim 1, where the charge pump is operable to receive the first and second reference signals from a voltage divider circuit.

3. (Previously Presented) The charge pump of claim 2, where the first and second reference signals are substantially the same.

4. (Previously Presented) The charge pump of claim 3, where each of the first and second reference signals are substantially half the supply voltage.

5. (Previously Presented) The charge pump of claim 2, where the voltage divider circuit comprise a plurality of interdigitized resistors.

6. (Previously Presented) The charge pump of claim 1, where the first and second reference signals are received from first and second voltage divider circuits.

7. (Previously Presented) The charge pump of claim 6, where the first and second reference signals are substantially the same.

8. (Previously Presented) The charge pump of claim 1, where the first reference signal includes a constant voltage level that is between minimum and maximum voltage levels of the first input signal.

9. (Previously Presented) The charge pump of claim 8, where the first reference signal includes a constant voltage level that is substantially equal to a midpoint of a voltage range of the first input signal.

10. (Previously Presented) The charge pump of claim 8, where the first complementary transistor switches on substantially when the first input transistor switches off and the first complementary transistor switches off substantially when the first input transistor switches on.

11. (Previously Presented) The charge pump of claim 10, where the second complementary transistor switches on substantially when the second input transistor switches off and the second complementary transistor switches off substantially when the second input transistor switches on.

12. (Cancelled)

13. (Previously Presented) The charge pump of claim 1 further comprising a biasing circuit that provides a biasing signal to gate terminals of the first and second discharging transistors.

14. (Previously Presented) The charge pump of claim 13 further including a second output terminal that is coupled to a filter that reduces coupled switching noise of at least one of the first reference signal and the second reference signal.

15. (Previously Presented) The charge pump of claim 14, where the filter comprises a transistors configured to provide capacitance and resistance.

16. (Previously Presented) The charge pump of claim 15, where the second output terminal connects with a voltage-to-current converter.

17. (Previously Presented) The charge pump of claim 1, where the first and second input transistors comprise switching transistors.

18. (Cancelled)

19. (Cancelled)

20. (Previously Presented) The charge pump of claim 1, where the charge pump operates with a supply voltage of less than 2.5 volts.

21. (Previously Presented) The charge pump of claim 20, where the charge pump operates with a supply voltage of less than 1.9 volts.

22. (Previously Presented) The charge pump of claim 20, where the charge pump has at most three transistors connected via source and drain terminals between the supply voltage and ground.

23. (Previously Presented) The charge pump of claim 1, where the signal at the first output terminal is substantially isolated from signal noise in the first and second control signals.

24. (Previously Presented) The charge pump of claim 23, where the signals at the first output terminal is substantially isolated from switching noise caused by the first and second input transistors.

25. (Previously Presented) The charge pump of claim 1 further comprising:

first and second charging transistors connected between a supply voltage and the first and second input transistors, respectively;

a voltage divider circuit that provides the first reference signal and the second reference signal to gate terminals of the first and second complementary transistors, where the first reference signal and the second reference signal are each substantially half the supply voltage;

third and fourth charging transistors connected between the supply voltage and the first and second complementary transistors, respectively;

a biasing circuit that provides a biasing signal to gate terminals of the first and second discharging transistors; and

a filter comprising transistors operable to reduce coupled switching noise at a second output terminal of the filter;

where the first complementary transistor switches on substantially when the first input transistor switches off and the first complementary transistor switches off substantially when the first input transistor switches on.

26 - 38. (Cancelled)